Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

A 115V, 400HZ AIRCRAFT INVERTER BASED ON CASCADED MULTILEVEL INVERTER TOPOLOGY WITH REDUCED CONDUCTING SWITCHES IN THE CURRENT PATH

[1]AHMAD SYUKRI MOHAMAD and [2]RUHAIDA ABDUL RASHID

[1]Electrical Engineering Section, Universiti Kuala Lumpur, British-Malaysian Institute, Batu 8, Jalan Sungai Pusu, Gombak, Selangor, Malayisa
[2]Avionics Section, Universiti Kuala Lumpur, Malaysian Institute of Aviation Technology, Jenderam Hulu, Dengkil, Selangor, Malaysia

ABSTRACT
The paper described the aircraft inverter in aircraft electrical systems, the various types of inverter designs and the simulation and experimental analysis of the proposed inverter. The aircraft inverter produces a rated 115V, 400Hz output that is only used in emergency situations primarily caused by loss of main electrical generation systems. But as the aviation world moving towards more electrical aircraft (MEA) and variable speed constant frequency (VSCF) electrical systems, the inverter role will not only limited to emergency power supply only but will be integrated in the main electrical generation system in the future aircraft. The cascaded multilevel inverter topology has the ability to increase the voltage output without the need of a transformer. Thus it offers the design with the space and weight reduction that are always desired in the aircraft systems design. Simulation results for the inverter circuits are given with the load set to up to 1kW, as the common rating for aircraft inverter. The inverter performance is analyzed based on the output waveforms and total harmonic distortions (THD) according to different number of cells and power switching devices used. To validate the simulation, an experimental hardware prototype is built and tested. The experimental results shown that the prototype inverter successfully produced the rated 115V, 400Hz inverter output with THD much less than the 5% limit set by IEEE and aircraft standards.
Keywords: aircraft inverter, cascaded multilevel inverter, minimum conducting switches

1. Introduction

In aircrafts, inverters are used to provide the emergency power to the aircraft during loss of normal electrical supply to the flight critical loads such as flight instruments, radio communications and navigation equipments. These systems are essential for a safe flight.

Although modern aircraft now equipped with ram air turbine (RAT) generator as another option for emergency power supply, the inverter remains a critical component in airborne standby power system. In the early days, rotary inverters were used. However this type of inverter produces noise and heavy. Modern aircrafts use static inverter that has no moving parts (Tooley & Wyatt,2018), thus longer operating life, lighter and considerably small in size.

With the advancement of the aircraft electrical technology, the inverter usage becomes more explored. One example is the variable speed constant frequency (VSCF), which has been used in MD-90 and Boeing 777. In this system, the variable frequency generator output is converted into direct current that put

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

through a dc link before converted back into constant 400 Hz, 115 V using a converter or inverter (Moir & Seabridge, 2018). In the proposed advanced aircraft power system for the future more electric aircraft (MEA), the role of inverter to provide constant frequency 400Hz, 115V electrical power become more significant. In order to supply constant frequency to the loads, the varying frequency generator output converted first into 270V dc power in the main dc busbar before converted back into constant ac power using inverter (Emadi, Ehsani & Miller, 2004).

The main challenge in every aircraft component design is the restricted space and load factor. The reduction in aircraft weight by reducing the components individual weight will definitely reduce the aircraft fuel consumptions(Capahart,2007; Kundu,2010). The direct result of this is the aircraft range can be improved and the reduced weight can be substituted with other financially commercial payload.

Figure 1.
A static inverter in a Boeing 757-200 aircraft

In most aircraft designs, there is only one inverter used in the emergency standby power supply system (see Figure 1). If anything happens that leads to the inverter failure during flight, the aircraft will be left without any emergency power supply. The fact that this possible incident is a real threat to aviation safety is described in one of the United States of America Federal Aviation Administration (FAA) Airworthiness Directives (AD). It is reported that one resistor in the inverter that is used in most of the Boeing models (737, 747, 757, 767 and 777) is prone to overheating and ignition, ultimately resulting the inverter failure. The AD states that;

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

"prior to 2003 there were 39 static inverter failures on 39 airplanes; since 2003 there have been 15 inverters on 15 airplanes that failed due to the R170 resistor overheating, and approximately 9,400 units have been manufactured"(Federal Aviation Administration Airworthiness Directives, 2010,pp. 1-9)
These aircrafts are widely used around the world, and with trans-oceans flights involving these aircrafts is almost unavoidable, the threat of losing emergency power is always present.
So it is thought that if the centralized inverter design is discarded in the future aircraft, the risk could be reduced. If inverters can be designed to be small, light and compact – perhaps each of the instrument, navigation and radio systems that supplied with inverter emergency power supply during loss of all generation system could be designed to be built in or co-located with each operating critical instruments.

2. Aircraft inverter types

There are various inverter designs that are used in aircraft systems since the World War II era. It could be vibrating contacts, mechanical chopper, rotary inverter or electronics inverter (Button,1943).The need for onboard inverter becomes prevalent during the 1940s as the aircraft instrument and radio systems demands rapidly increased. This is because all these instruments use ac current while the main aircraft power supply at that time comes from 28V dc generator (Hayes & Ray, 1954).
There are several popular aircraft inverter designs. Each has its own advantages and disadvantages. But it is always the main interest in the design of these inverters, apart from high efficiency and low harmonic content; is the factor of space consumption and weight. The space and weight factor could not be neglected as it will directly affect the aircraft payload factor and fuel consumption (Capahart,2007; Kundu,2010).

2.1 Rotary type inverter

The most popular type of inverter before the advance development of power electronics devices are the rotary type inverter. The rotary inverter basically is an AC generator being driven by a dc motor. Usually a four-pole compound Dc motor output shaft is connected to the shaft of a star-wound ac generator (Tooley & Wyatt,2018).
The main advantage of this type of inverter is that the output sine power is clean and harmonic free, as the AC current is produced by an AC generator itself. There are no need for an output filter or output transformer, as it usually in case with many of static inverter systems. But the rotary type inverter is heavy, and produces noise due to the constant moving motor and generator. It also needs constant checks and a lot of maintenance, especially the motor and generator commutator brushes. The brushes easily wear out particularly during high altitude operation (Hayes & Ray, 1954), as in the case of aircraft flying condition.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

This will increase the risk of inverter failure, and it also increases the cost; mainly the component replacement cost and maintenance cost.

2.2 Static inverter

As the power electronics devices becomes more efficient and popular, static inverters start to replace the old rotary inverters. The static inverter is desirable because it has no moving parts, hence the name 'static'. Because it has no moving parts, the inverter becomes quieter and most importantly, smaller and lighter. There also no more wearing commutator brushes, so it can has a longer life while reducing maintenance time and cost.

One of the simplest static inverter is the oscillator based inverter. A 400Hz oscillator is connected to the dc supply and producing low voltage ac current. The oscillator output voltage then stepped-up using a power transformer (Tooley & Wyatt, 2018). But the current capability of an oscillator circuit is limited. To increase the output power of the inverter, high power switching devices are used. The most common power electronics switching devices are bipolar junction transistor (BJT), field effect transistor (FET), insulated gate bipolar transistor (IGBT), silicon controlled rectifier (SCR), gate turn-off thyristor (GTO), TRIAC and MOSFET. To increase efficiency of the power electronics devices, instead of using it in the active region (as the case in power amplifier), the devices are used in the saturation and cut-off region, namely as an on-off configuration (as a switch). This is because, the efficiency of the devices are greatly improved in this configuration (up to over 90%), known as class D amplifier (Boylestad & Nashelsky, 1999).

Gourash and Birchenough (1970) apparently used this principle in their design of aircraft 400Hz, 115V inverter. The inverter used pulse width modulation (PWM) technique to maximize the efficiency of the inverter. It also claimed to reduce the inverter weight in large amount compared to other designs at that time (1970). This design has shown that it eliminates the need for the transformer to increase the output voltage, as in the earlier design. As a result, the inverter weight is greatly reduced, and the efficiency in increased. However, some of the prevalent issues in the PWM inverter are the high switching rate of the switches that causes significant switching losses(Batarseh,2011) and also high harmonics content in the output (Vazquez& Lopez, 2018)

Aircraft inverters (onboard and ground services) that use PWM switching strategy are described in various technical papers (Macellari et al.,2006; De Maglie et al.,2009;Qun-Min et al.,2009; Basile et al.,2000; Zhu et al., 2009; Housheng et al.,2010).There are also inverters that use multilevel topology, with PWM switching to refine the output waveform (Homeyer et al.,1997; Liu et al.,2008; Liu et al.,2009; Chun-Xi et al.,2009).But the cascaded multilevel inverter technology that described in (Homeyer et al.,1997; Liu et al.,2008; Liu et al.,2009; Chun-Xi et al.,2009), was limited to 5-level output waveform (two cascaded cell). It is interesting to see what happen if a cascaded multilevel inverter (or cascaded

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

multicell inverter) design is used at a higher level number to operate at 400Hz, 115V output; because based on the papers discussed above, there are no such experiment done yet.

3. Cascaded multilevel inverter

The cascaded multilevel H-bridge inverter is based on the concept of full bridge (or popularly known as H-bridge) switch cell modules that are connected in series sequentially one by one in order to create a staircase waveform that imitates a sinusoidal waveform. Each module can produce a positive output voltage and a negative output voltage in a magnitude similar to the input source or cell dc voltage, as well as a zero output voltage (Mohamad & Mariun, 2016). The advantage of this type of power inverter is, when the output voltage level is increased to a suitable higher value, it can produce an output that is almost resembles the clean sinusoidal output waveform. The staircase output waveform produced by multilevel inverter helps to reduce lower level harmonics while increasing power quality. It also reduces the voltage stress of each individual power switching devices.

Multilevel inverter design concept is where cascaded dc power supplies are connected using semiconductor power switches to synthesize a staircase or stepped voltage waveform. There are several advantages of this design compared with two-level inverter that uses high frequency switching as in the case of PWM technique (Khomfoi et al.,2007; Corzine,(2002); Rodriguez,2002)– the staircase waveform quality means that the output voltage is generated with very low distortion, reduce dv/dt stress and also electromagnetic compatibility (EMC), smaller common mode (CM) voltage therefore reduce the stress on the bearings of a motor connected to a multilevel inverter, and, low distortion in input current drawn by the multilevel inverter.

Multilevel inverter also can operate in both fundamental switching frequency and high PWM switching frequency. Higher switching frequency however, as in the case of PWM inverter will produce higher switching losses (Khomfoi et al.,2007; Corzine,(2002); Rodriguez,2002).

Other cascaded multilevel inverter advantages are the number of possible output voltage levels is more than twice the number of dc sources (Khomfoi&Tolbert,2007) and the higher number dc sources or cells are used, the blocking voltage (OFF voltage) requirement of each power switches become smaller – allowing a lower voltage rating power switches used.

One of the disadvantages of the multilevel H-bridge is the high number of power switching devices needed in each design (Khomfoi & Tolbert,2007). The number of power switches needed increases according to the number of levels of the intended output waves. So, in order to get an output wave that is as close as possible to a clean sine wave, the design will need a lot of power switches especially if H-bridges are used in the design. For each cell, the design needs

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

four power switches. So, for an 11-level output (5-cells), 20 power switches needed.

Babaei and Hosseini (2009) proposed a topology that claims to reduce the number of power switches needed. In the proposed topology, only two power switches needed for each cell, plus four cells (a H-bridge) at the output terminals to reverse the polarity (in order to create the negative side of a sine wave output). So, by using this topology, for an 11-level output (similar case as above) needed only 14 switches (10 cell switches plus 4 for H-bridge output). For higher level output, the four output H-bridge switches will become only a small fraction of the total switches needed.

However, Mohamad et al (Mohamad, Mariun, Sulaiman & Radzi, 2014) proposed a better topology that not only reducing the number of total switches but also the number of conducting switches. For an 11-level output version, only 10 switches needed (6 cell bidirectional switches, 4 for H-bridge output) and only 4 conducting switches in the current path. Amazingly, for 20 cells, 41-level circuit version (where the THD level safely below the required 5% limit), the total switch count is 25, but the number of conducting switches is maintained at 4.

4. The proposed aircraft inverter circuit design process

The aircraft inverter circuit shown in Figure 2 adopted the cascaded multilevel inverter topology proposed by Mohamad et al (2014) as the design featuring the least number of power switches compared to the conventional H-bridge topology. It also has the lowest conducting switches in the current path, thus reducing the internal loss in the aircraft inverter – increase the inverter efficiency and more importantly reducing the risk of overheating as stated in (Federal Aviation Administration Airworthiness Directives, 2010, pp. 1-9)

The MOSFET is selected as the power switches as it has faster switching time compared to other devices in order to accommodate higher aircraft electrical system frequency of 400Hz compared to domestic utility frequency of between 50 to 60Hz.The cells are switched on according to the bidirectional MOSFET switching sequence from M_0 (for 0V output), then M_1 on, then M_2on, then M_3 on until $M_n$on (for peak voltage, V_{peak}) then the sequence reverse back from M_n to M_1 to M_0 (0V).

Whenever any of the conducting bidirectional MOSFET is switched on, all other MOSFET pair must be switched off. While H-bridge MOSFET H_1 and H_2 switched on for half-cycle period to produce the positive sequence of the output sine wave, and MOSFET H_3 and H_4 are switched on for another half-cycle period for the negative sequence of the output sine wave.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

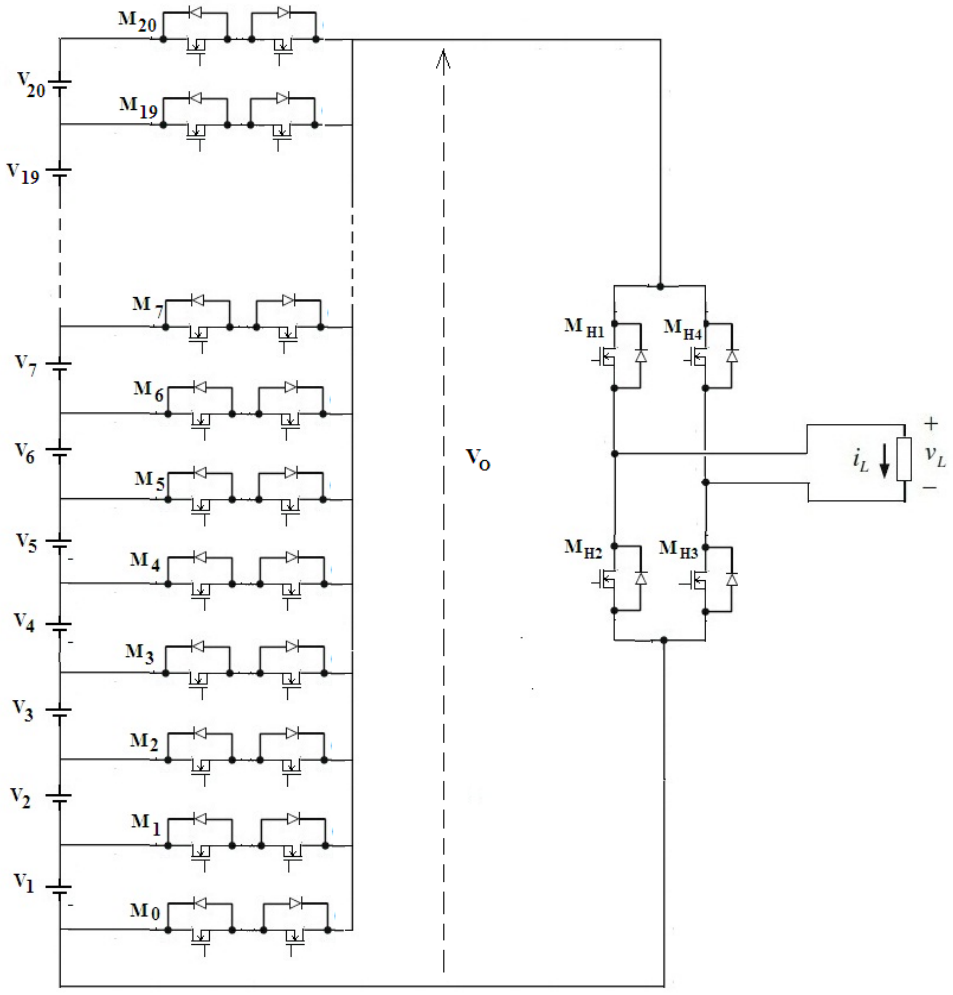

Figure 2. The proposed aircraft inverter circuit

The aircraft electrical rated voltage is $115V_{rms}$, so the peak output voltage for the inverter is

$$V_{peak} = V_{rms} \times 1.414 \quad (1)$$
$$= 162.61V$$
$$\approx 162V$$

The number is round up to 162V instead of 163V for ease of calculation when the voltage is divided into smaller independent voltage sources.

The peak voltage then divided with the n number of cells of the inverter to get the voltage value for each cell

$$V_1 = V_2 = V_3 = \ldots\ldots\ldots = V_n = V_{peak} \div n \quad (2)$$

It is important to note that in order for the stepped-wave produced by the inverter to as close as possible imitate the sine wave, the on time for each cell is critical. The cells voltages will be added up with each other starting with the V_1, V_2 and so

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

on until V_n, before the sequence reversed with V_n is then taken out of the output circuit, then V_{n-1} and so on until lastly V_1 is out so that the output voltage goes back to 0V. For the negative cycle of the sine wave the sequence start again with the H-bridge reversing the output polarity.
In order to achieve this, the on time for each of the cell is set at the time when the equivalent sine wave voltage reaches half of the cell voltage plus the previously switched on cells in the sequence as shown in Figure 3.

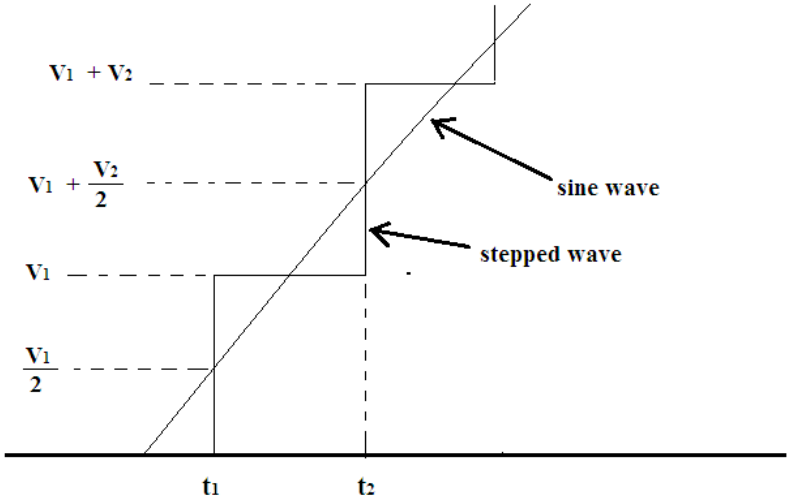

Figure 3.
The cell switching time in order to create the stepped-wave that follows closely the fundamental sine waveform shape

So, the respective MOSFET that control the on time of the cell is switched on when the 'invisible' fundamental sine wave 'intercepts' the stepped-wave at half the voltage of the respective cell to be on.
The sine wave equation is given as

$$v(t) = V_{peak} \sin 2\pi ft \quad (3)$$

With the peak voltage for the design is 162V and frequency of the system is 400Hz, the equation becomes

$$v(t) = 162 \sin 800\pi t \quad (4)$$

From Figure 3 we could see that at t_1, inverter output voltage will be $V_1 \div 2$, so

$$v(t_1) = 162 \sin 800\pi t_1 = V_1 / 2 \quad (5)$$

Solving for t_1, the equation will becomes

$$t_1 = [\sin^{-1} \{(V_1 / 2) \div 162\}] \div 800\pi \quad (6)$$

While for t_2

$$v(t_2) = 162 \sin 800\pi t_2 = V_1 + V_2 / 2 \quad (7)$$

Solving for t_2, the equation will becomes

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

$$t_2 = [\sin^{-1}\{(V_1 + V_2 / 2) \div 162\}] \div 800\pi \quad (8)$$

So, it can be concluded that the equation for t_n is

$$t_n = [\sin^{-1}\{(V_1 + \ldots + V_{n-1} + V_n / 2) \div 162\}] \div 800\pi \quad (9)$$

5. Simulation results

The simulation is done by using MATLAB Simulink. There are five inverter circuits simulated with no load condition – 3-cells, 5-cells, 10-cells, 15-cells and 20-cells cascaded multilevel inverter, in order to get the best total harmonic distortion (THD) reading according to aircraft standard. The THD requirement for an aircraft ac power as stated in widely used MIL-STD-704F aircraft electrical standard is it must be lower than 5% (maximum distortion factor 0.05) (US Department of Defense, 2004, pp.1-38), although European Aviation Safety Agency (EASA) adopted 7% maximum limit for an airborne static inverter (European Aviation of Safety, 2003, pp.1-8).

The simulation results are shown in Figure 4, 5, 6, 7 and 8. It is presented that the 20-cell inverter configuration has the best no-load THD reading at 1.980%. Although 10-cell inverter THD reading is 3.898% is within the standard required, it is best to choose a lower value as when the inverter is connected the loads, the THD reading maybe pushed above the allowed limits due to noise from the load operations.

The results also show that the 20-cell inverter configuration is closely resembles the sine wave with all cells have an individual voltage rating of 8.1V (refer equation (2)).

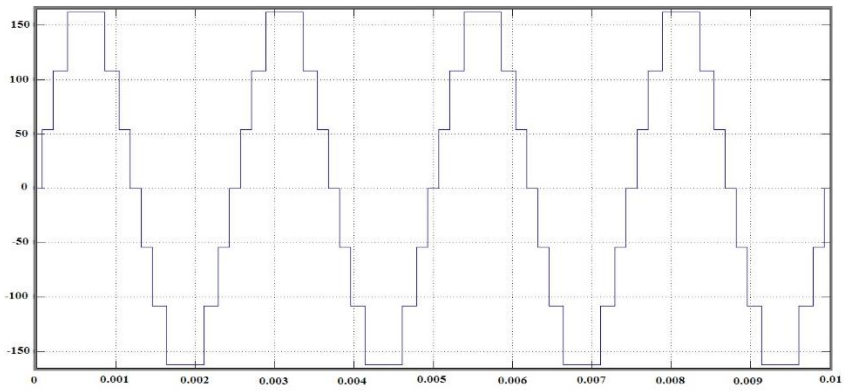

Figure 4. Output voltage waveform for 3-cells cascaded multilevel inverter

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

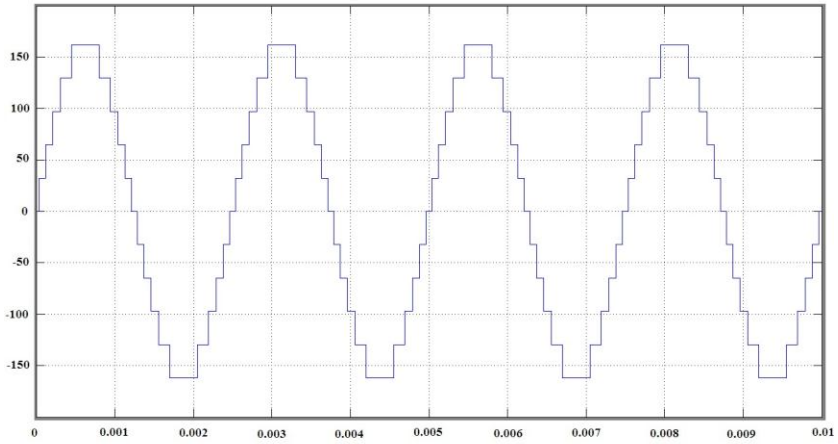

Figure 5. Output voltage waveform for 5-cells cascaded multilevel inverter

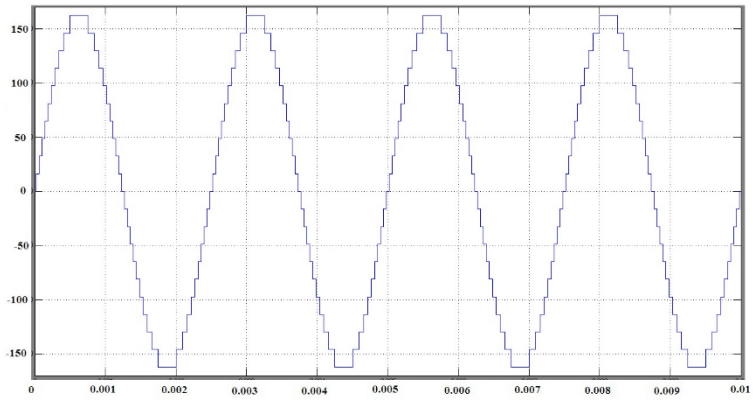

Figure 6. Output voltage waveform for 10-cells cascaded multilevel inverter

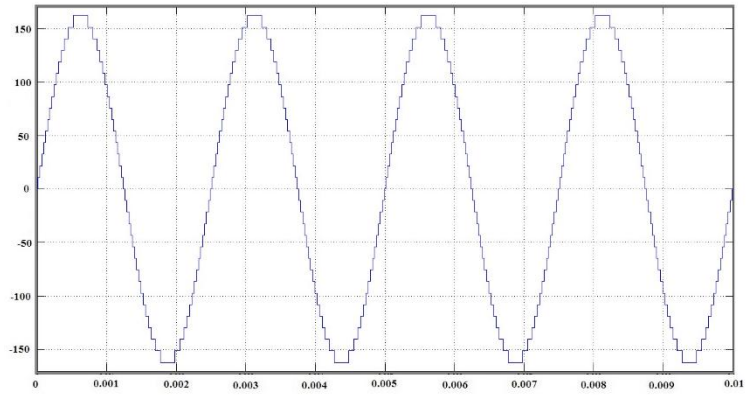

Figure 7. Output voltage waveform for 15-cells cascaded multilevel inverter

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

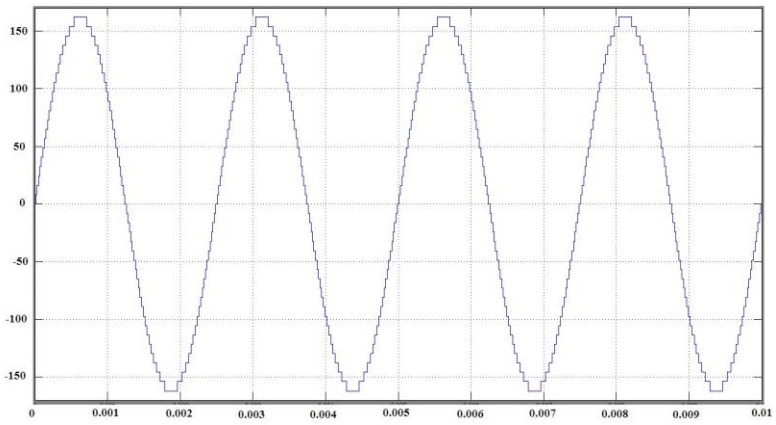

Figure 8. Output voltage waveform for 20-cells cascaded multilevel inverter

Table 1. Inverter output voltage (no load condition) THD percentage according to number of cellsin each inverter

Number of cells	THD (%)
3	12.230
5	7.587
10	3.898
15	2.625
20	1.980

The inverter performance shows a considerable change in output voltage when connected to the load (see Table 2). In this respect, the 20-cells, 41-level inverter suffers when the output voltage drops significantly when connected to a 1kW load. This is because when current flows through a MOSFET, there will be voltage drop (IR_{ON}) across the MOSFET due to drain-to-source resistance, R_{DS}. Since the current will flow through 40 MOSFETs in conventional H-bridge 41-level inverter, the internal voltage loss is very significant (Figure 9). This situation can be rectified if the inverter built using topology that has minimum conducting switches in the current path(low cumulative R_{DS} on-state resistance), as proposed and shown in Figure 2.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

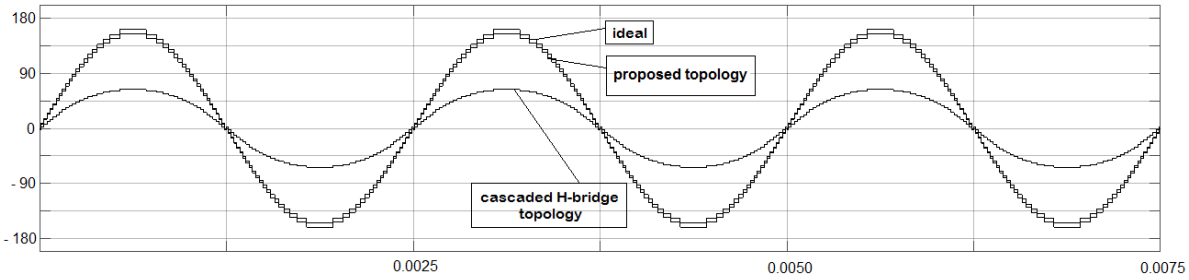

Figure9.
The effects of conducting switches count in the conventional cascaded H-bridge inverter and the proposed inverter circuit

Table 2. The effect of load on the 41-level inverter performance

Topology	**10W**		**100W**		**1kW**	
	$V_{o(rms)}$	THDv	$V_{o(rms)}$	THDv	$V_{o(rms)}$	THDv
Ideal	115.0 V	1.98 %	115.0 V	1.98 %	115.0 V	1.98 %
Proposed inverter	114.7 V	1.98 %	114.0 V	1.99 %	110.1 V	2.00 %
Cascaded H-bridge	113.2 V	2.65 %	100.4 V	2.54 %	47.5 V	5.56 %

Table 2 shows also that THD measurements for the prototype inverter voltage output only slightly changes when the load varies from no-load condition up to 1kW. For the inverter configuration with constant number of conducting switches, the load increment from the no-load condition to up to 1kW did not has any significant effects on the THD reading. However, for a topology that has variation in the conducting switches count such as two per level increment in the topology in (Babaei& Hosseini, 2009),the THD measurement for 20-cells inverter has the most THD measurement increment of more than 0.8%, as shown in Table 3, compared to only 0.2% in the proposed topology (Table 2).

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

Table 3.
The effect of load variation on the inverter output voltage THD (%) for topology with variation of conducting switch count increment of two for each level increase

Number of cells	Inverter Load		
	No-load	**100W**	**1kW**
3	12.230	12.220	12.130
5	7.587	7.574	7.479
10	3.898	3.882	3.897
15	2.625	2.611	2.940
20	1.980	1.972	2.782

6. Experimental hardware results

A prototype inverter based on 41-level new cascaded multilevel inverter topology is built. There are three main components of the prototype inverter – the main inverter circuit, the MOSFETs drivers and FPGA. The cascaded cells switches in the main inverter circuit are built on printed circuit board (PCB) modules, with 5 units of switches on a single module. The H-bridge is built on a separate PCB. The MOSFETs drivers also built on PCB with 5 units of drivers on a single module. The MOSFETs are FQP22N30.

Each of the cascaded cells switches, H-bridge switches, the MOSFETs drivers and FPGA are tested for their functional operations before connected together in a complete full inverter assembly to make sure each component are functioning correctly. After all the components and modules are verified for their functionality, they are assembled together.

With all the separate circuit parts of the prototype inverter circuit is tested and verified to be functioning correctly, they then were put together into a full hardware assembly for the overall test and inverter output test. The prototype inverter full hardware assembly output test set up is shown in Figure 10 and Figure 11.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

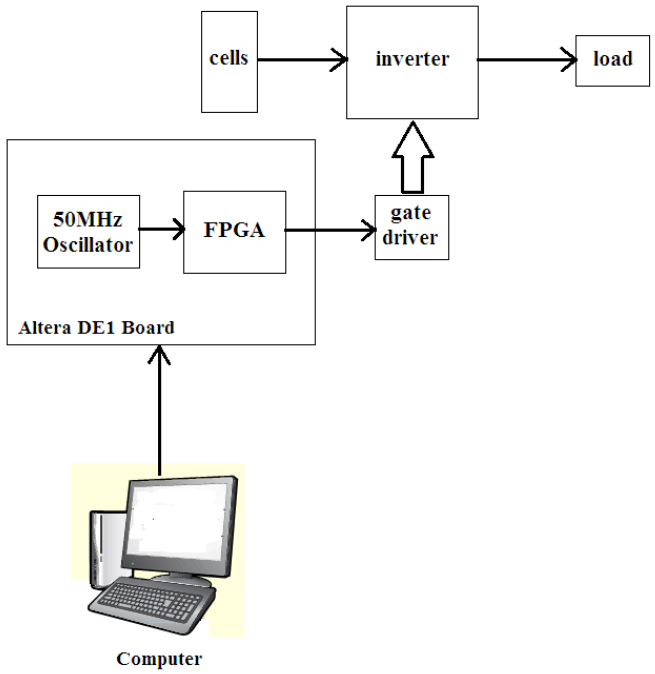

Figure10. The prototype inverter full hardware assembly output test set up

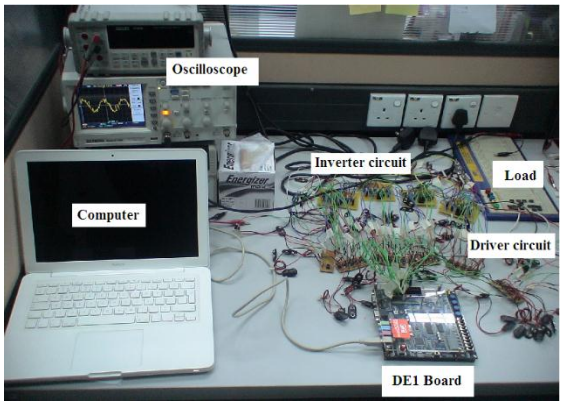

Figure 11. The prototype inverter experimental set up on the test bench

The prototype inverter is then tested with a series 790Ω, 68mH resistive-inductive (RL) load. The power factor of the load at 400Hz is 0.977. The hardware experimental test result resembles the simulation result, with the THD reading for the load voltage, VL, is 2.532%, compared to 2.002% for the simulation load voltage waveform (Figure 12). The THD reading for this test is well below the 5% THD limit requirements for aircraft standards and IEEE standard 519-2014.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

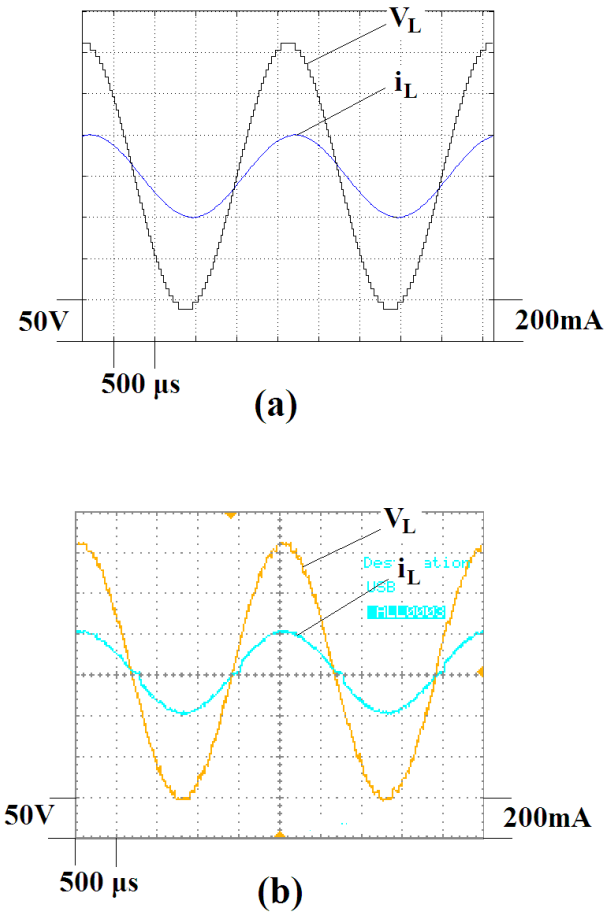

Figure 12. Inverter output with 790Ω, 68mH load; a) simulation; b) experimental result

7. Conclusion

The simulation results show that the cascaded multilevel inverter topology has a potential to be used for the aircraft inverter design. All the inverter configurations have been tested with load conditions almost similar to the actual aircraft inverter load (most aircraft inverter has 1kW rating). The THD measurement shows that a 10-cells configuration and above can achieved the desired THD performance as required by the IEEE and aircraft standards. However a 20-cells, 41-level inverter has much better performance and safer THD level, particularly for critical loads such as in the aircraft.

The prototype 41-level inverter was successfully tested both in simulation and experimental for its function and viability. The prototype inverter output is a well-defined 41-level sinusoidal stepped voltage waveform with peak voltage of 163V and rms voltage of 115V. The frequency is 400Hz. The prototype inverter was tested with resistive-inductive (RL) load, and it succeeded to produce input with a very low distortion level as well as almost resembles a clean sinusoidal waveform.

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

The prototype inverter was experimented with 790Ω, 68mH load. The THD level for the loads are 2.532%, below the 5% limit set out in IEEE standard 519-2014. The only issue that must be addressed by future design is how to create multiple independent cells in the aircraft electrical system to accommodate the proposed design, as the current technology only provided the aircraft inverter with a single dc supply through a 28Vdc battery. The modification in aircraft battery system will eventually results in modification in the battery charging system, and this will open an opportunity for a new study.

References

Babaei, E., & Hosseini, S. H. (November 2009). Energy Conversion and Management: New cascaded multilevel inverter topology with minimum number of switches (Vol.50, Issue 11,pp.2761-2767).

Basile, G. L., Buso,S.Fasolo,S., Tenti,P., &Tomasin,P. (2000). Industry Applications Conference Record of the 2000 IEEE: A 400 Hz, 100 kVA, digitally controlled UPS for airport installations (Vol. 4, pp. 2261-2268).

Batarseh, I. (2011). *The power of MOSFET*. In Rashid M.H. (Ed), *Power Electronics Handbook* (3rd ed., pp. 43-71). *Butterworth-Heinemann*

Boylestad, L., &Nashelsky,L. (1999). Electronic Devices and Circuit Theory (7th ed.,pp. 679-714). Prentice-Hall Inc.

Button, C.T. (1943). American Institute of Electrical Engineers : Aircraft Inverter Construction (Vol. 62, Issue 9, pp. 598-602).

Capehart, B.L. (2007).Encyclopedia of Energy Engineering and Technology (pp.26-29). CRC Press.

Chun-xi,L., Wei-ming,M., Chi,S., & Wen-hua,H. (2009). Asia-Pacific Power and Energy Engineering Conference: Research on Harmonics Suppression in High Power Middle Frequency 400Hz Inverter (pp.1-4).

Corzine,K. (2002). *Multilevel Converters*. In Skvarenina T. L.(ed.), *Industrial Electronics Series: The Power Electronics Handbook* (pp. 6.1-6.23). *CRC Press.*

De Maglie,R., Osvald,G., Engstler, J., Engler, A. &Carayon, J. P. (2009). European Conference on Power Electronics and Applications: Optimized 70kW power inverter dedicated to future aircraft applications (pp. 1-10).

Emadi,A., &Ehsani, M. (2004).Vehicular Electric Power Systems: Land, Sea, Air and Space Vehicles (pp. 231-238). Marcel Dekker, Inc.

European Aviation Safety Agency (EASA). (24 October 2003). Certification Specifications for European Technical Standard Order, Static Electrical Power Inverter.

Federal Aviation Administration Airworthiness Directive. (February 1, 2010). Electrical Power - Static Inverter Resistor - Modification / Replacement (No. US-2009-26-03).

Gourash,F., &Birchenough, A.G. (1970). NASA Technical Note: Design Analysis and Performance of a 2.5 kVA Static Iverter Pulse-Width-Modulated (NASA TN D-5586).

Hayes, C.P., & Ray, L.L. (1954). American Institute of Electrical Engineers: 400-Cycle Inverters for Military Aircraft (Vol. 64, Issue 5, pp. 233-237).

Homeyer, W. G., Bowles, E. E. Lupan, S. P., Walia, P. S., Maldonado, M. A. (1997). Proceedings of the 32nd Intersociety. Energy Conversion Engineering Conference: Advanced power converters for More Electric Aircraft applications (Vol.1,pp. 591-596).

Housheng,Z., Yanlei,Z. &Haidong,Li (2010). 2nd International Conference on Computer Engineering and Technology: Design of three-phase intermediate frequency aviation power based on single chip microcomputer (Vol 4, pp. V-669-V4-672).

Jilin Daxue Xuebao (Gongxueban)/Journal of Jilin University (Engineering and Technology Edition)
ISSN：1671-5497
E-Publication：Online Open Access
Vol: 40 Issue: 12-2021
DOI 10.17605/OSF.IO/8YCWF

Khomfoi,S., & Tolbert, L.M. (2007). *Multilevel Power Converters*. In Rashid, M. H. (ed.) *Power Electronics Handbook* (pp.451-482). *Academic Press.*

Kundu, A. (2010). Cambridge Aerospace Series: Aircraft Design. Cambridge University Press

Liu,C., Ma,W. Sun,C. &Hu,W. (2009). IEEE 6th International Power Electronics and Motion Control Conference: Research on digital control design of high power middle frequency 400Hz inverter power (pp. 1544-1549).

Liu,C., Sun,C. &Hu,W. (2008). International Conference on Electrical Machines and Systems: Proportional-resonant controller of high power 400Hz inverter in stationary frame (pp.1772-1777)

Macellari,M., Grasselli,U., &Schirone,L. (2006). Aerospace Conference: An on-board inverter controlled by the waveform switching technique.

Mohamad, A.S. & Mariun,N. (2016). IEEE International Conference on Power and Energy (PECon): Simulation analysis of an improved cascaded multilevel inverter topology (pp.178-181).

Mohamad,A.S., Mariun,N., Sulaiman,N. &Radzi, M. A. M. (2014). IEEE Innovative Smart Grid Technologies – Asia: A new cascaded multilevel inverter topology with minimum number of conducting switches (pp.164-169).

Moir,I.,&Seabridge,A. (2008). Aircraft Systems: Mechanical, electrical, and avionics subsystems integration (3rd ed., pp. 153, 192-230).John Wiley & Sons Ltd.

Qun-min,Y., Yan-dong,Shi., Ning-fei., & Yi, F. (2009). WRI World Congress on Computer Science and Information Engineering: The Modeling and Simulate for Aircraft Secondary Electric Power Supply Based on Saber (Vol.2, pp. 218-222).

Rodriguez, J., Lai, J. & Peng, F. Z. IEEE Transactions on Industrial Electronics: Multilevel Inverters: A Survey of Topologies, Controls, and Applications (Vol.49, No.4, pp.724-738).

Tooley,M. (2018). Aircraft Electrical and Electronic Systems (2nd ed., pp.133-142). Routledge (Taylor & Francis Group).

USA Department of Defense. (12 March 2004). Aircraft Electric Power Characteristics (MIL-STD-704F).

Vázquez,N & López,J.V. (2018). *Inverters*. In Rashid M.H. (Ed), *Power Electronics Handbook* (4th ed., pp. 289-338). *Butterworth-Heinemann*

Zhu,H., Li,Y., Li, Z. &Wang,P. (2009). Asia-Pacific Power and Energy Engineering Conference: Design and Performance Analysis of High Power Static 400-Hz Supply (pp.1-4).